

WHAT IS CLAIMED IS:

1. A printed circuit board comprising:
a plurality of stacked layers; and
a via extending through said stacked layers, said via
5 including a plated through hole located within a
predetermined number of said stacked layers and a back-
drilled hole located within the remaining stack layers,
wherein said plated through hole without an electrically
conductive material located on walls therein has a diameter
10 that is substantially the same size or smaller than a
diameter of said back-drilled hole.

2. The printed circuit board of Claim 1, wherein at
least one layer of said stacked layers includes a plane
15 layer.

3. The printed circuit board of Claim 1, wherein at
least one layer of said stacked layers includes a signal
layer.
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4. The printed circuit board of Claim 1, wherein a
plurality of said vias are located within said printed
circuit board.
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5. A method for forming a plated through hole in a multi-layered printed circuit board, said method comprising the steps of:

drilling a first hole having a first diameter through
5 said printed circuit board;

drilling a second hole having a second diameter concentrically around and through a predetermined depth of said first hole in said printed circuit board;

plating said second hole and a remaining portion of
10 said first hole in said printed circuit board; and

back-drilling a third hole having a third diameter concentrically around and through the remaining portion of said plated first hole to remove that portion of said plated first hole and leave said plated second hole which
15 forms the plated through hole in said printed circuit board.

6. The method of Claim 5, wherein said second diameter of said second hole is substantially the same size
20 or smaller than said third diameter of said third hole.

7. The method of Claim 5, wherein said step of plating includes applying a layer of conductive material on walls of said second hole and on walls of the remaining
25 portion of said first hole and on predetermined areas on a top surface and bottom surface of said printed circuit board.

8. The method of Claim 5, wherein said printed circuit board has a plurality of said plated through holes formed therein.

5 9. A printed circuit board comprising:
a plurality of stacked layers; and
a plated hole located within a predetermined number of
said stacked layers that was formed by:

drilling a first hole having a first diameter
10 through said stacked layers;

drilling a second hole having a second diameter
concentrically around and through a predetermined
depth of said first hole;

plating walls of said second hole and walls of a
15 remaining portion of said first hole within said
stacked layers; and

back-drilling a third hole having a third
diameter concentrically around and through the
remaining portion of said plated first hole to remove
20 that portion of said plated first hole and leave said
plated second hole which forms the plated through
hole.

10. The printed circuit board of Claim 9, wherein at
25 least one layer of said stacked layers includes a plane
layer.

11. The printed circuit board of Claim 9, wherein at least one layer of said stacked layers includes a signal layer.

5 12. The printed circuit board of Claim 9, wherein said second diameter of said second hole is substantially the same size or smaller than said third diameter of said third hole.

10 13. The printed circuit board of Claim 9, wherein said step of plating includes applying a layer of conductive material on the walls of said second hole and on the walls of the remaining portion of said first hole and on predetermined areas on a top surface and bottom surface
15 of said stacked layers.

14. The printed circuit board of Claim 9, wherein a plurality of said plated through holes are formed within said printed circuit board.

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